

V1.4 07/18/2012

Generalpius	,															
Customer								Date								
Project Titl	е							Code	No.							
Project Des	scriptio	n														
CPU Worki	ng Volta	age (VD	D) 🗆 2	.7V ~ 3	.6V			I/O V	oltage)		_2	.7V ~ 3	3.6V		
CPU Opera	ition Fre	equency	,	ck cont U opera			(MHz	Value	writte	n to 0x	7007),		stal 768Hz)	_ C	heck
LCD Config	guration	1	Mod Bit- LCI	de: □C per-pixo D Buffe	Gray Le el: □ r can o	evel 1 🔲 Inly loc		no (Bla	ack & \ // (0x4)	White) 000~0>	(477F)		V _{LCD} :			heck
LCD Driver	ame (*.ts	sk):	Fra List LCI Car LCI If M a. N b. C LCI	me Rate SEG Concentration only under Segment Single Multi-Chilland Make succentration of Drive	e: Control mon: se GP nent: Chip Sol hip Solu ip Solu ure to to use G	Hz Regist L16800 olution lution tion: urn off PL168 ponents	GPL16 001A bui GPL16 001A bui S:	D31 It-in C 68001 8001A uilt-in FPLD S FPLC S Others FFF"	OM Dr A) A built-i SEG69 Series Series for un	in VLCI Solution	D charg G73. dy no: _ dy no: _ dy no: _ area)	x7033 COM)	np.			heck heck heck
User ROM check sum: (Reported by G+IDE tool) SRAM size: 4K words (0x00000~0x0FFF)																
DPRAM size: 1920 Words (0x4000~0x477F)																
Input / Output																
IOA Port	b1E	h14	h12	h12	h11	h10	b0	ho	h7	b.c.	b.E	h4	h2	h2	h1	hO
Input	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4_	b3	b2	b1	b0
Output																
Wakeup																
Special Function		TimerA CCP	EXTB												OMMC [63:61]	
Used																



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Input	Certeralpus																
Input	IOB Port																
Output Wakeup Spei	b15 b14 b1			3 b	b12 b11		10 b9) b8	b7	b6	b5	b4	b3	b2	b1	b0	
Wakeup Special SPI	Input																
Special Function	Output																
Function	Wakeup																
Used IOC Port	Special					S	PI									alog	
DC Port	Function					CLK, I	00, DI								Inputs		
Input	Used																
Input Output Wakeup Special Function WRE MWE IRRX IRTX CS1 DISP ON Dedicated I/O SCK SD Used Working Reset) URX IRTX CS1 DISP ON Dedicated I/O SCK SD Used Working Reset) Disable Enable: (2.0V) LVR (Low Voltage Reset) Disable Enable: (2.2V 2.4V 2.6V 2.8V) Internal Memory In emulation mode setup (Value written to 0x704C) Configuration Released mask code setup (Value written to 0x704C) This value must be greater than 0x0001 and must be verified on EMU system. External Memory (CS0) Disable Enable: Start Address: End Address: Fixpe: SRAM ROM FLASH Others Size: Access Time: CS0 control register: End Address: End Address: Type: SRAM ROM FLASH Others Size: Access Time: CS0 configuration CS1 CS1 control register: (Value written to 0x7020)	IOC Port							_									
Output Wakeup Special MRE MWE URX UTX CS1 DISP Dedicated I/O SCK SD.		b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Wakeup Special MRE MWE URX UTX CS1 DISP Dedicated I/O SCK SD. Used URX IRTX US4 US5 US6 U	Input																
Special Function MRE MWE MRE	Output																
LVR (Low Voltage Reset)	Wakeup																
LVR (Low Voltage Reset)	Special	MDE	N/N/⊏			URX	UTX	CS1	DISP			Jedicat				SCK	SDA
LVR (Low Voltage Reset)	Function	WIIVE	10100			IRR	(IRTX	001	ON		- -	- I	.00 1/0	1		OOK	ODA
LVR (Low Voltage Reset)	Used																
LVD (Low Voltage Detector)																	
Internal Memory Configuration Released mask code setup (Value written to 0x704C) This value must be greater than 0x0001 and must be verified on EMU system. External Memory (CS0) Configuration Disable Enable: Start Address: End Address: Type: SRAM ROM FLASH Others Size: Access Time: CS0 control register: (Value written to 0x7020) External Memory (CS1) Configuration Disable Enable: Start Address: End Address: Type: SRAM ROM FLASH Others Size: Access Time: CS1 control register: (Value written to 0x7021)	LVR (Low	Volta	ge Res	et)													
Configuration Released mask code setup (Value written to 0x704C) This value must be greater than 0x0001 and must be verified on EMU system. External Memory (CS0) Disable	LVD (Low Voltage Detector)			□Disable □Enable: (□2.2V □2.4V □2.6V □2.8V)													
This value must be greater than 0x0001 and must be verified on EMU system. External Memory (CS0)	Internal Memory				In emulation mode setup (Value written to 0x704C)												
External Memory (CS0) Disable	Configuration				Released mask code setup (Value written to 0x704C)												
External Memory (CS0) Disable					This value must be greater than 0x0001 and must be verified on EMU system.												
Configuration Type: SRAM ROM FLASH Others Size: Access Time: (Value written to 0x7020) External Memory (CS1) Configuration Disable Enable: Start Address: End Address: End Address: Type: SRAM ROM FLASH Others Size: Access Time: (Value written to 0x7021)	External Memory (CS0)				□Disable □Enable: Start Address: End Address:												
Size: Access Time: (Value written to 0x7020) External Memory (CS1) Configuration Disable Enable: Start Address: End Address: End Address: Type: SRAM ROM FLASH Others Size: Access Time: (CS1 control register: (Value written to 0x7021)																	
CS0 control register: (Value written to 0x7020) External Memory (CS1) Configuration CS0 control register: (Value written to 0x7020) Type: SRAM ROM FLASH Others Size: Access Time: CS1 control register: (Value written to 0x7021)												•					
External Memory (CS1) Configuration Disable Enable: Start Address: End Address: Type: SRAM ROM FLASH Others Size: Access Time: CS1 control register: (Value written to 0x7021)										_			4- 0v70)20\			
Type: SRAM ROM FLASH Others Size: Access Time: (Value written to 0x7021)																	
Size: Access Time: CS1 control register: (Value written to 0x7021)	External N																
CS1 control register: (Value written to 0x7021)	Configura	Type: □SRAM □ROM □FLASH □Others															
					Size: Access Time:												
					CS1 control register: (Value written to 0x7021)												
CS1 timing control register: (Value written to 0x7024)	CS1 timing control register: (Value writt								vritten	to 0x70)24)						
A/D Interface Disable Enable:	A/D Interf																
If Enable, please check following		If Enable, please check following															
Module Used:																	
☐ Microphone																	
if used, Auto Gain Control:																	
☐ Analog Input(s)																	
If used, A/D Line_In inputs (CHC,CHD shared with IOB[1:0]) voltage range											ange						
							_v ~ _		V	,							



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Generalplus							<u>v</u>	1.4 07/10/201	
UART	□Disable	□Enab							
	If Enable, M			te =	—				
IrDA	□Disable	□Enab							
	If Enable, M				一				
SEG[0:7] Used as key scan ou	•		□Yes			f yes, please check L0	CD brightne		
SEG[8:15] Used as key scan o	utput		Yes	□No)			☐ Check	
Watchdog enable (Software Wi	•	-						□Yes □No	
If watchdog is enabled, please	<u></u> .								
Watchdog port (\$700BH) must	☐Check ☐Check								
All functions must be verified or	All functions must be verified on the EMU board or EMU chip system.								
		Ma	ask Cod	e Optic	on				
EMUSEL0 code option as:							<u> </u>	□ 0	
EMUSEL1 code option as:							<u> </u>	<u> </u>	
IROMEN code option as:							□ 1	□ 0	
ADBUSEN code option as:							□ 1	□ 0	
Protect code option as:							□ 1	□ 0	
		General F	Program	ming (Ch	necklist			
is the customer's responsibility for any non-checked box even to conditions are met and verified	this confirma					•	-		
All used SRAM must be initializ	zed after pov	ver on (St	trongly re	<u>comm€</u>	ıen	nded).		☐Check	
Make sure the used SRAM variables are not over stack reserved area.								☐Check	
Make sure the Interrupt section is located in the page0 or is declared as .TEXT section (\$08000-\$0FBFF).								Check	
(A)Make sure no current leakage in I/O or speaker amplifier during sleeping.								□Check	
(B) Make sure all I/Os are not floating during sleeping.								□Check	
To avoid abnormal wake up in sleep mode, users should disable the interrupt of all sources with 32768Hz clock.							□Check		
This code has been running sta	and-alone.				_			□Check	
Non-used I/O ports must be masked off (for input process).							□Check		
Example, if IOA[0:7] are input: R1 = [P_IOA_Data]; ; Read I/O port A Data									
l	R1 & = 0x00	FF;	; Mask	k higher	r b	oyte			
(CMP R1,0	x0011;	; Lowe	r byte is	is a	available for compare	operation		
		Do	ocument	Version	on	1			
To make sure the correct version	on of docum	ent is use	-— ∍d, pleas	e fill ou	ut t	the followings:			
(A).GPL168001A Programming	g Guide Vers	sion							
(B). μ'nSP™ IDE User Manual	Title and Ve	ersion							
(C).Other documents (if any)									



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Development Too	ol / Board Version								
To make sure the correct version of hardware is used, pleas	se fill out the followings:								
(A).Emulation Board Version									
(B).Emulation Chip Version									
(C).Piggyback Version(if used)									
(D).Others (if any)									
To make sure the correct version of software is used, please	e fill out the following:								
(A). μ'nSP™ IDE Version									
(B).SACM Library Version(if used)									
(C).Others (if any)									
Speech Lib	rary Usage								
Generalplus speech libraries is applied in this code	□Yes □No								
If yes, which kind speech have used									
☐ A1600 ☐ A2000 ☐ A3200 ☐ A3200-2 channel ☐ A2000 Encode ☐ MS01									
□ S200 □ S240 □ S480/720 □ S530 □	S600								
Does speech algorithm allocate in page 0		□Yes □No							
For Third Part	ty Application								
Cyberon voice recognition solution is applied in this code		□Yes □No							
If yes, please fill out the followings:		ļ							
(A). Types of solutions: □SI only □SD only □SID(bot	th SI & SD) □SV								
(B). VStar Modeling Toolkit IDE Version									
(C). VStar Library Version: BSRVlib									
(D). VStar-SDK Programming Guide Version									
(E). Others (if any)									
Customer Note	GENERALPLUS Note								
Name (print): Tel:	Name (print):Tel:								
Signature:	Signature:								

Note: Please send/fax this form to GENERALPLUS. GENERALPLUS will return it back with signature.